AMENDMENTS TO THE CLAIMS

Please amend claims 21, 24, 26, 42, 43, 47 and 49 as follows:

1-20. (Canceled)

21. (Currently Amended) A method for manufacturing semiconductor devices, the method comprising:

providing a semiconductor wafer with a ~~wafer~~ front surface having a plurality of circuit elements formed thereon, wherein the semiconductor has a back surface opposite to the front surface;

forming on the ~~wafer~~ front surface a plurality of electrodes connected to the circuit elements;

inserting the wafer into a burn-in apparatus;

testing the circuit elements in the burn-in apparatus for electrical functions, through the electrodes, with the back surface of the wafer exposed to convective air in the burn-in apparatus; and

dividing the wafer into a plurality of semiconductor devices.

22. (Previously Presented) A method according to claim 21, wherein said dividing includes dividing the wafer after said testing.

23. (Previously Presented) A method according to claim 22, further comprising:

mounting the wafer on a circuit board with an elastic sheet interposed therebetween, including electrically connecting wiring circuits on the circuit board to the electrodes on the wafer through conductive elastic portions of the elastic sheet.

24. (Currently Amended) A method according to claim 23, further comprising:

disposing over the back surface of the wafer a holding plate having a through hole; and

pressing the wafer on the circuit board with the holding plate.

25. (Previously Presented) A method according to claim 22, further comprising:

mounting the wafer on a circuit board with a film interposed therebetween, including electrically connecting wiring circuits on the circuit board to the electrodes on the wafer through bump electrodes in the film.

26. (Currently Amnded) A method according to claim 25, further comprising:

disposing over the back surface of the wafer a holding plate having a through hole; and pressing the wafer on the circuit board with the holding plate.

27. (Previously Presented) A method according to claim 21, further comprising the step of forming a plurality of solder balls as the electrodes.

28-41. (Canceled)

42. (Currently Amended) A method according to claim 24, further comprising providing the convective air over the back surface of the wafer through the through hole.

43. (Currently Amended) A method according to claim 26, further comprising providing the convective air over the back surface of the wafer through the through hole.

44. (Previously Presented) A method for manufacturing semiconductor devices, the method comprising:

preparing a semiconductor wafer with a first surface and a second surface, the second surface being opposite to the first surface, wherein the first surface has a plurality of circuit elements formed thereon;

forming a plurality of electrodes on the first surface, the electrodes being connected to the circuit elements;

inserting the semiconductor wafer into a burn-in apparatus;

testing the circuit elements in the burn-in apparatus for electrical function, through the electrodes, with the second surface of the semiconductor wafer exposed to convective air in the burn-in apparatus; and

dividing the semiconductor wafer into the plurality of semiconductor devices.

45 (Previously Presented) A method according to claim 44, wherein the dividing includes dividing the semiconductor wafer after the testing.

46. (Previously Presented) A method according to claim 45, further comprising mounting the semiconductor wafer on a circuit board with an elastic sheet interposed therebetween, including electrically connecting wiring circuits on the circuit board to the electrodes on the semiconductor wafer through conductive elastic portions of the elastic sheet.

47. (Currently Amended) A method according to claim 46, further comprising:

disposing over the second surface of the semiconductor wafer a holding plate having a through hole; and

pressing the semiconductor wafer on the circuit board with the holding plate.

48. (Previously Presented) A method according to claim 45, further comprising mounting the semiconductor wafer on a circuit board with a film interposed therebetween, including electrically connecting wiring circuits on the circuit board to the electrodes on the semiconductor wafer through bump electrodes in the film.

49. (Currently Amended) A method according to claim 48, further comprising:

disposing over the second surface of the semiconductor wafer a holding plate having a through hole, and

pressing the semiconductor wafer on the circuit board with the holding plate.

50. (Previously Presented) A method according to claim 44, further comprising forming a plurality of solder balls as the electrodes.

51. (Previously Presented) A method according to claim 47, further comprising providing the convective air over the second surface of the semiconductor wafer through the through hole.

52. (Previously Presented) A method according to claim 49, further comprising providing the convective air over the second surface of the semiconductor wafer through the through hole.

REMARKS

The Examiner's Office Action mailed on May 7, 2003 has been received and its contents carefully considered.

Claims 21-27 and 42-52 are pending in this application. Claims 21, 24, 26, 42, 43, 47 and 49 are amended herein.

The Examiner's withdrawal of the previous final rejection of the pending claims is noted with appreciation.

In the present Action, the Examiner has rejected claims 21-27 and 42-52 under 35 USC 103(a) as being obvious over Nakata et al. (U.S. Patent No. 6,297,658) in view of Budnaitis et al. (U.S. Patent No. 5,896,038). Except to the extent addressed by the amendments herein to the claims, the rejection is respectfully traversed.

As recited in amended claim 21, the present invention includes providing a semiconductor wafer with a front surface having a plurality of circuit elements formed thereon, forming on the front surface a plurality of electrodes connected to the circuit elements, and testing the circuit elements in a burn in apparatus for electrical functions, through the electrodes, with the back surface of the wafer exposed to convective air in the burn-in apparatus. Similarly, independent claim 44 recites a method that includes preparing a semiconductor wafer with a first surface and a second surface, wherein the first surface has a plurality of circuit elements formed thereon, forming a plurality of electrodes on the first surface, the electrodes being connected to the circuit elements, and testing the circuit elements in a burn-in apparatus for electrical function, through the electrodes, with the second surface of the semiconductor wafer exposed to convective air in the burn-in apparatus.

The Nakata reference cited by the Examiner does generally disclose burn-in testing of semiconductor devices at the wafer level conducted in a burn-in cassette by connecting electrically the bumps 17 on the probe card 12 to the electrode pads 16 formed on the surface of the semiconductor wafer 10. However, as the Examiner acknowledges in the Office Action, Nakata fails to disclose exposing the rear surface of the semiconductor wafer 10 to air circulating through convection while the semiconductor wafer 10 is mounted in the wafer tray 11. In fact, Nakata discloses that the spaces 15 and 25 are evacuated so as to bring the wiring board 13 closer to the wafer tray 11 and thereby assure

good contact with the electrode pads 16 through the probe card 12. Hence, there is little, if any, air available in the Nakata invention to circulate by convection.

To overcome the deficiency in the Nakata reference, the Examiner asserts that Budnaitis discloses (see Figures 2-3) providing a semiconductor wafer (1) with a surface having a plurality of circuit elements (chips 2) formed thereon, inserting the wafer (1) into a burn-in apparatus (6) wherein the wafer (1) is exposed to convective air in the burn-in apparatus (6) (see column 8, lines 41-54). Further, according to the Examiner, Budnaitis teaches that the addition of the wafer exposed to air is advantageous because it provides temperature control of the wafer during testing in the burn-in apparatus. The Examiner argues that it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Nakata by adding means to blow air on the wafer as taught by Budnaitis in order to control the temperature the wafer during testing in the burn-in apparatus.

The applicant respectfully disagrees. The text in Budnaitis referenced by the Examiner (column 8, lines 46-48) discloses that "... the wafer may be cooled by blowing cold air over the wafer, [or] by including a cooling elements in the chuck 15..." However, Budnaitis fails to disclose cooling by exposing the back surface of the wafer to convective air in the burn-in apparatus, as the rejected claims require. The forced air circulation suggested in Budnaitis is significantly different from the convective cooling claimed in the present invention. Moreover, both Nakata (see Figure 1) and Budnaitis (see Figure 3) disclose that the back of the semiconductor wafer, when mounted in the burn-in apparatus, is pressed against a solid surface. Hence, neither of the references teaches or suggests exposing the back surface to convective air in the burn in apparatus, as the rejected claims require. Obviously, combining the references, as the Examiner suggests, will not cure this deficiency.

For at least these reasons, it is respectfully submitted that independent claims 21 and 44, as well as their respective dependent claims, patentably distinguish over the applied art references, whether considered individually or a combination.

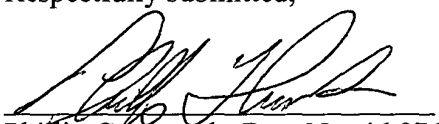
Further, it is respectfully submitted that that the dependent claims recite features that independently distinguish over the applied art combination. For example, claims 24, 26, 47 and 49 recite "disposing over the back (second) surface of the semiconductor wafer

a holding plate having a through hole," and claims 42, 43, 51 and 52 recite "providing the convective air over the back (second) surface of the wafer through the through hole." It is respectfully submitted that neither Nakata nor Budnaitis discloses this feature of the present invention. In the Action, the Examiner points to the through hole 26 in the probe card 12 of Nakata. However, it is clear from Figure 1 of Nakata that, at best, this hole could admit air to the front surface of semiconductor wafer 10, but not to the back surface, as required.

The Examiner's rejection of the claims having been fully addressed, it is submitted that the application, as amended, is in condition for allowance. Notice of such, with allowed claims 21-27 and 42-52, is earnestly solicited.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,



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Date

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